Design and Realization of a Millimeter-Wave Si/SiGe HBT Frequency Multiplier

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***Abstract*— In this paper, the design of an active millimeter-wave frequency doubler using an Si/SiGe heterojunction bipolar transistor (HBT) as the active device is studied. Simulations are made using a developed physics-based large-signal model for Si/SiGe HBT's, which includes thermal dependence. Despite the high-output operating frequency of the fabricated doubler being close to $f_{\max}$ 67 GHz for the Si/SiGe HBT, the conversion efficiency in a not completely optimized circuit is found to be better than -12 dB. The 3-dB bandwidth for the doubler is approximately 7.4%. These results are found to be comparable to a heterojunction field-effect transistor (HFET) doubler operating equally close to its $f_{\max}$. Simulated results of the doubler performance with varied terminating impedances for the HBT are presented as design aids.**

I. Introduction

THE objective for investigating silicon-based (monolithic) microwave integrated circuit [(M)MIC] technology is the inherent possibility to realize millimeter-wave single-chip systems having advanced signal-processing capabilities. Silicon-based active devices such as Si/SiGe heterojunction bipolar transistors (HBT's) have shown great potential of performance where devices with a maximum frequency of oscillation $(f_{\max})$ of 70 GHz have been implemented in circuits, and $f_{\max}$ of 160 GHz has been reached recently in common emitter configuration for single devices [1], [2]. Moreover, high-resistivity silicon, which is the substrate material for millimeter-wave SiGe-based circuits, has been shown to give dielectric losses within the same order as semi-insulating GaAs at millimeter-wave frequencies [3].

In order to evaluate the feasibility of the SiGe technology for applications at millimeter-wave frequencies, demonstrators are being designed. A first demonstrator chosen for evaluation of the silicon-based (M)MIC technology is a 55-GHz frequency multiplier using an HBT as the active device, having an $f_{\max}$ of 67 GHz. The frequency multiplier provides the opportunity to evaluate not only the application, but also nonlinear models developed for the millimeter-wave SiGe HBT's. The majority of designs of active millimeter multipliers are based on FET devices as the nonlinear component [4]–[6]. A frequency multiplier for lower microwave frequencies using an AlInAs/GaInAs/InP HBT was recently presented, showing promising results [7]. As far as the authors know, no frequency multiplier for millimeter waves has been presented using an SiGe HBT as the active device.

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II. HBT Model

A large-signal model whose parameters can be directly related to the physical transistor has been developed for nonlinear applications. A modified Ebers–Moll model having transit time delay added to the current generator has been shown to sufficiently model HBT transistors at microwave frequencies [8]. The model has the benefit of taking into account the physical properties of the transistor and of having only a moderate number of parameters. Also of importance is that the variation of the technological parameters such as layer structure and geometries of the device can be accounted for.

The implementation of the model has been done in a SPICE-like simulator using a Microwave Design System (MDS) from Hewlett-Packard. A special feature in MDS called the symbolically defined device (SDD) has been used for modeling the intrinsic part of the transistor, schematically shown as the shaded part of Fig. 1(a).

For simplicity and computational speed, the model has been divided into three levels, each describing one part of the actual transistor where the lowest level mainly accounts for pad and contacting parasitics, using only linear elements. The middle level describes extrinsic parasitic resistances and reactances, some of which are bias dependent.

The highest level models the intrinsic part of the transistor (see Fig. 1(a), shaded part), where the aim has been to use elements that give a discrete analogy to the electrical processes occurring. For this reason, separate diodes are used in each junction to model the ideal electron and hole injection currents (I_{eF}, I_{eR}) and (I_{hF}, I_{hR}), respectively, where the indexes e, h, F, and R denote electrons, holes, forward, and reverse currents, respectively [see Fig. 1(a)]. As a result, α_F and α_R for

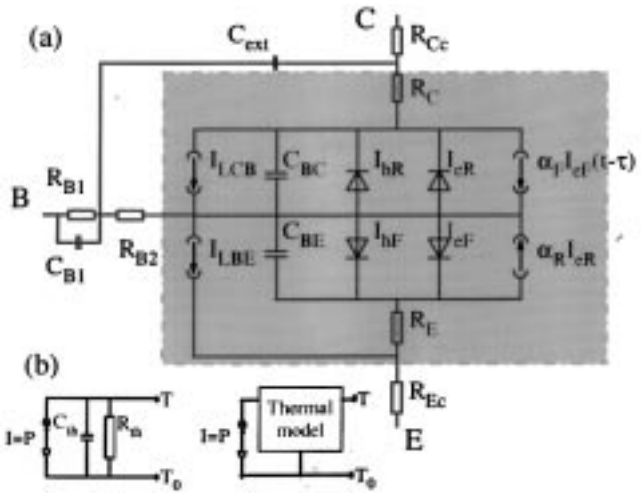

Fig. 1. Large-signal HBT model. (a) Electrical model. (b) Examples of thermal equivalents for the circuit.

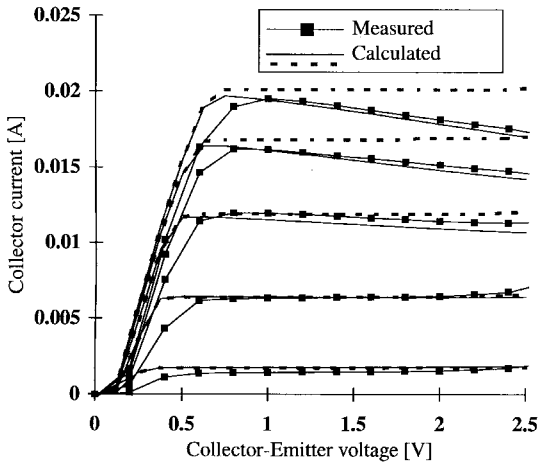

Fig. 2. Measured and calculated *I–V* characteristics for a $1 \times 20\ \mu\text{m}^2$ device varying I_B from 50 to 250 μA. Dotted line shows calculation without a thermal model, straight line shows calculation with thermal model.

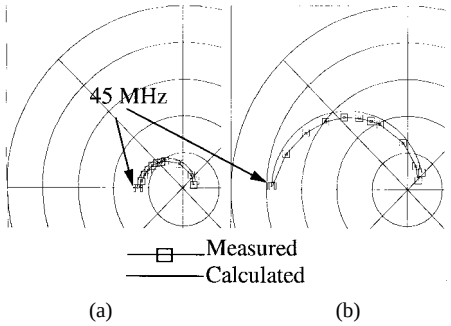

Fig. 3. Measured and calculated forward transmission (S_{21}) from 45 MHz to 50 GHz. DC bias is (a) 3 V, 1 mA and (b) 3 V, 10 mA. Full scale of the plots are 10. Pointed out in the graph is the starting frequency.

the current generators in Fig. 1(a) do not need to account for electron injection efficiency, which makes electrical modeling of thermal effects less complex. Since the electron and hole injections exhibit different thermal dependence due to different bandgaps in the different layers, a separate treatment of these currents makes any function describing their interdependence in a unified diode superfluous. The current generators I_{LCB} and I_{LBE} have been added to empirically model high injection effects and the surface currents occurring on a mesa device structure. The capacitances C_{BE} and C_{BC} have been calculated using the SPICE model for junction depletion capacitances, taking into account charge compensation in the collector space charge region which occurs at high collector currents for the base–collector capacitance C_{BC} [9].

Thermal modeling has been accomplished by creating an interface via the SDD, making it possible to use different complexities in the thermal model; from a lumped thermal resistance to nonlinear models derived from FEM simulations, see Fig. 1(b). In this application, a lumped structure like the one in Fig. 1(b) is sufficient for finding the correct bias point.

The analytical expressions which the model parameters are based on are useful for a first estimation of transistor behavior. Starting values for the parameters are calculated from given device geometries, layer structure, and known semiconductor properties. However, due to the complexity in the physical relations governing the semiconductor, and to uncertainties in the fabrication process, some of these parameters that are used in the calculations inherently contain errors. Extraction and fitting of some model parameters to measured data is, therefore, necessary.

The measurements, performed at a known ambient temperature, result in Gummel *I–V* plots and S-parameter curves at different bias. It is desirable to measure the S-parameters at low and high collector current and at least one intermediate value to get information of transistor behavior at the most important bias levels.

The fitting of parameters is done in a two-step process. Initially, only the technological parameters are allowed to vary within limits known from the fabrication process. Following this first step, elements in the equivalent circuit that do not directly relate to the intrinsic transistor are varied to further improve the accuracy of the model.

Parameters relating to nonidealities in the transistor-like leakage currents occurring on the surfaces of the collector and emitter and the base current at high injection have been extracted to achieve good agreement with measured dc characteristics. Additionally, certain resistors and time delays of the current generators are adjusted to best fit the measured S-parameters.

In order to verify the model, the electrical characteristics were calculated for a 1 μm $\times$ 20 μm emitter-area HBT with device geometry and layer structure similar to the one described in [10].

With some necessary adjustment of technological parameters due to inherent variations in the fabrication process, the resulting *I–V* characteristics and S-parameters have been calculated and compared to measurements (see Figs. 2 and 3). As can be seen, the simulated results agree with both the dc and RF measurements. The slightly sharper kink for simulated *I–V* characteristics in Fig. 2 at low V_{CE} and high I_C compared to the measured data is likely caused by a quasi-saturation creating a base pushout effect occurring when the base–collector junction is forward biased [11]. The typical decrease in β at high I_C with increasing V_{CE} is caused by the self-heating

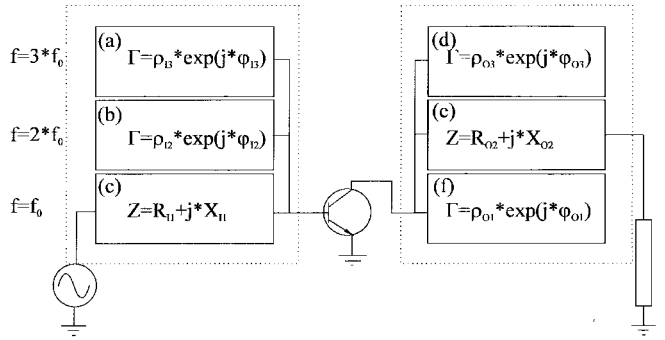

Fig. 4. A schematic presentation of the MDS model for the ideal doubler, which is used for optimization of matching circuit. Each block denotes one S-parameter block (shown with a shaded "S").

TABLE I
NOMINAL VALUES FOR OPTIMIZATION PARAMETERS IN DOUBLER STRUCTURE (SEE FIG. 4)

Parameter	Value	Parameter	Value
R_{I1} [Ω]	19.7	ρ_{O1}	0.964
X_{I1} [Ω]	42.7	φ_{O1} [°]	90.0
ρ_{I2}	0.830	R_{O2} [Ω]	57.8
φ_{I2} [°]	221	X_{O2} [Ω]	217

effect [9]. For comparison, the *I–V* characteristics have also been calculated without a thermal model ($R_{\rm th}$ in Fig. 1(b) is set to zero) (see Fig. 2). The S-parameters are verified for a variation in collector current of one order of magnitude, thus making large-signal modeling plausible.

III. MULTIPLIER SIMULATION AND DISCUSSION

The simulation model for the doubler (see Fig. 4), developed in MDS, consists of separated ideal loads for the different frequencies of interest, i.e., fundamental, second, and third harmonic, respectively. The loads have been realized either as impedances or as reflection coefficients. The impedance coefficients have been used on the input for the fundamental frequency and on the output for the second harmonic [see Fig. 4(c) and (e)]. The latter have been used when a reactive low-loss termination is desirable [see Fig. 4(a), (b), (d), and (f)].

The process of designing the passive circuitry around the transistor has consisted of two conceptual steps, which have been iterated to find an as optimal design as possible. In the first step, ideal impedances/reflection coefficients (described above) have been used. They have been optimized using assumptions that the circuit should as efficiently as possible match the transistor to 50 Ω on the input at the fundamental frequency and on the output at the second harmonic. Further, the input should block the second harmonic and the output should block the fundamental frequency.

In the second step, the calculated optimum impedances/S-parameters for the input and output circuits have been used for deriving a matching circuit using 50-Ω transmission lines shunted by shorted and open stubs. Since the resulting circuit does not exactly have the same characteristics as the ones found in the first step, it is necessary to recalculate the ideal input matching circuit of the multiplier, setting the impedances on the output to the ones found in the second step. Further

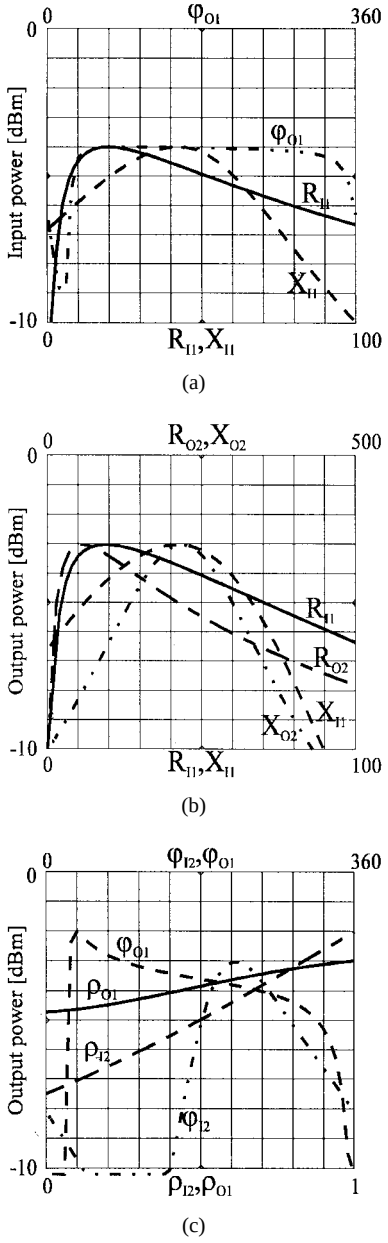

Fig. 5. Impact on input and output power from variation of matching parameters. One parameter was varied at a time. During optimization, source power was set to -4 dBm. (a) Input power as a function of R_{I1}, X_{I1}, and φ_{O1} (see Fig. 4). (b) Output power as a function of R_{I1}, X_{I1}, R_{O2}, and X_{O2} (see Fig. 4). (c) Output power as a function of ρ_{O1}, ρ_{I2}, ϕ_{O1}, and ρ_{I2} (see Fig. 4).

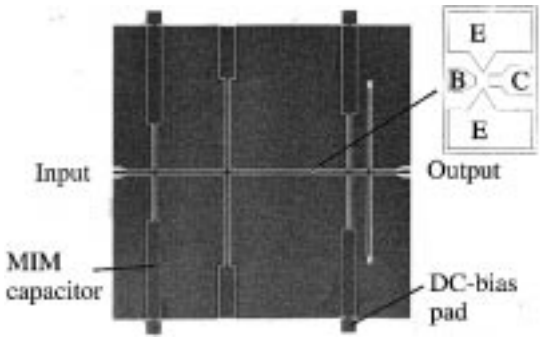

Fig. 6. The fabricated doubler circuit. A schematic of the transistor is shown on the right.

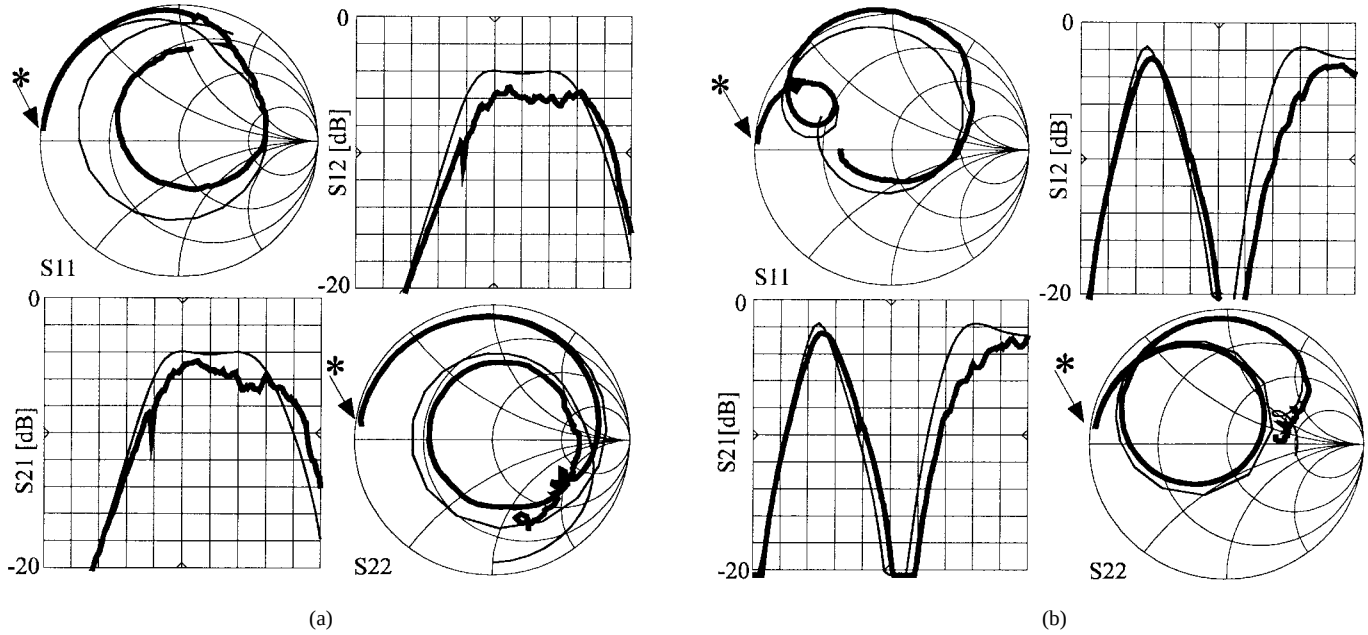

Fig. 7. Measured and calculated S-parameters for input and output matching circuit of the doubler circuit. Thin lines denote calculated data and thick lines denote measured data. The arrows in the Smith charts point out starting frequency. (a) Input structure, port 2 connecting to transistor. f = 1–50 GHz. (b) Output structure, port 1 connecting to transistor. f = 1–50 GHz.

iterations, e.g., optimizing the output with given impedances on the input, did not improve the overall performance.

In the simulations, the impact from the terminations on the performance of the doubler has been studied by varying each of these around their nominal value in the optimized structure, keeping other parameters fixed at their optimal values (see Table I).

In doing so, it can be noticed that they either affect input matching or output power, but only some parameters affect both. This has been a great advantage when performing optimizations since fewer parameters have needed to vary for each goal function. As can be seen in Fig. 5(a), the input absorbed power is affected only by the input source impedance (see Fig. 4), and by the phase (φ_{O1}) of the reflection on the output, at the fundamental frequency. If the phase (φ_{O1}) can be kept away from the region where it strongly degrades input matching, it can be allowed to vary rather freely, having only moderate impact on the output power [see Fig. 5(c)]. Input matching is sensitive to the input impedance on the fundamental frequency and extra care needs to be taken not to have too low a resistive part, since this clearly deteriorates performance.

The variation in input match as a function of ρ_{I2}, ρ_{I3}, ρ_{O1}, and ρ_{O3} (see Fig. 4) was found to be negligible due to small coupling between the harmonics and the fundamental frequency.

The output power [see Fig. 5(b) and (c)] also exhibits a clear dependence on the terminating impedances. Both the output match of the second harmonic and the input matching of the fundamental frequency obviously has a strong impact. The input matching has a similar dependence on the output power as on the absorbed input power [see Fig. 5(a) and (b)].

It can be seen that output power is very sensitive to variations in the reflection coefficient at the second harmonic [see Fig. 5(c)] on the input—both regarding magnitude and phase. It can also be seen that the reflection coefficient at the fundamental frequency on the output affects the output power. Similar dependence of the reflection coefficients at the input and output has been found for FET's [12]. Finally, the simulations show that the impact from the third harmonic is negligible both on input and output power, and thus, they need not be considered during optimization.

In the design currently employed (see Fig. 6), the input uses two matching stubs (shorts) and the output structure consists of a matching stub (short) for the second harmonic frequency and a filter (open) to block the fundamental frequency. The matching circuit on the input and output also presents the HBT with the optimum terminating impedances for the fundamental and second harmonic frequency, respectively. The short circuit is accomplished with MIM capacitors, thus making it possible to feed dc bias for the transistor on the center conductor of the coplanar waveguide.

To ensure a good understanding on how to realize the passive structures (shorts, opens, crosses, and MIM capacitors), test circuits have been designed and fabricated using electromagnetic (EM) field simulators from Hewlett-Packard.[1] Results from measurements on the passive structures conform well with simulated data up to at least 40 GHz (current limit of the measurement equipment used) (see Fig. 7).

IV. Measurements

The measurement setup for the evaluation of the fabricated doubler is comprised of an HP8510C vector network analyzer for S-parameter measurements. A synthesized sweeper,

[1]High-Frequency Structure Simulator (HFSS) and Momentum from Hewlett-Packard Corporation, Santa Rosa System Division, Santa Rosa, CA.

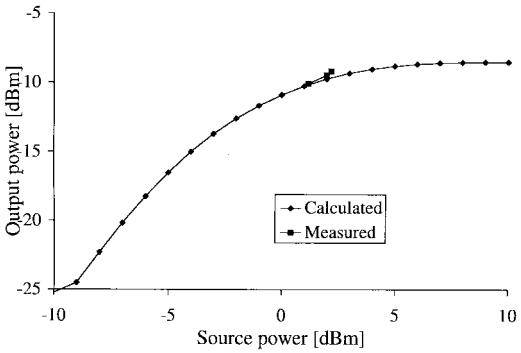

Fig. 8. Measured and calculated output power at 54.5 GHz versus source power at fundamental frequency for the doubler circuit.

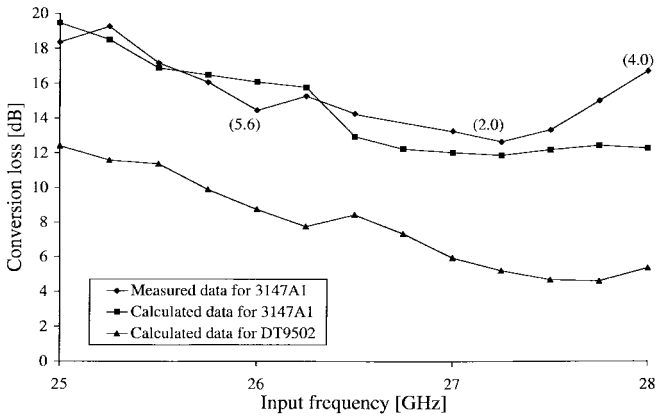

Fig. 9. Conversion loss versus frequency for the doubler circuit. Numbers within parenthesis depict source power at the input.

together with a power amplifier, was used for the power measurements. The circuit was contacted on the input and output side using coplanar probes. The output power was measured using a waveguide V-band power sensor in order to further suppress the fundamental frequency being below the cutoff frequency of the waveguide. Measurements with the power amplifier setup using a through line instead of the doubler showed no detectable output signal at the harmonic frequency, thus showing that power delivered at the second harmonic only originated from the doubler itself.

The measured frequency doubler showed a conversion efficiency of better than -12 dB at an input power of 1.2 dBm and a dc bias of 4 V and 3 mA (see Fig. 8). It is to be observed that the efficiency calculated is defined as measured output power versus source power, thus the efficiency is better than the one showed, taking into account mismatch on the input and output of the doubler. These results are found to be comparable to a heterojuncton field-effect transistor (HFET) doubler operating equally close to its $f_{\max}$ [4]. The 3-dB power bandwidth for the multiplier was measured to be approximately 7.4% (see Fig. 9). The multiplier was originally designed for an Si/SiGe HBT (here, called DT9502) having a different doping profile, thus having somewhat different S-parameters compared to the device used (here, called 3147A1), which was available at the time of implementation. The difference in S-parameters between the devices implied that the device used (3147A1) is not optimally matched for working in this frequency multiplier. The effect of this difference in transistor behavior can be seen in Fig. 9, where the doubler structure has been simulated using both the DT9502 and 3147A1 as the active device. Fig. 9 shows the calculated conversion efficiency for the doubler using the derived HBT model and the calculated impedances for the input and output embedding circuits. The good agreement between theory and experiments makes it possible to predict the conversion behavior for different HBT devices and improving the design of the doubler.

V. Conclusion

A frequency doubler for 55 GHz with a conversion efficiency of better than -12 dB, operating at an output frequency near $f_{\max}$ for the device, has been designed and realized.

We have also presented a physics-based large-signal Si/SiGe HBT model, which uses data given from the fabrication process for finding the model parameters. By fitting of a few parameters, it is possible to accurately model the large-signal behavior up to millimeter-wave frequencies, which has been shown with the simulated and designed doubler circuit.

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References

[1] F. Beißwanger, U. Güttich, and C. Rheinfelder, "Microstrip and coplanar SiGe-MMIC oscillators," in *Proc. 26th European Microwave Conf.*, Prague, Czech Republic, Sept. 1996, pp. 588–590.

[2] A. Schüppen, U. Erben, A. Gruhle, H. Kibbel, H. Schumacher, and U König, "Enhanced SiGe heterojunction bipolar transistors with 160 GHz $f_{\max}$," *IEEE Int. Electron Devices Meeting (IEDM'95) Tech. Dig.*, New York, Dec. 1995, pp. 30.4.1–30.4.4.

[3] J.-F. Luy, K. M. Strohm, H.-E. Sasse, A. Schüppen, J. Buechler, M. Wollitzer, A. Gruhle, F. Schäffler, U. Guettich, and A. Klaaβen, "Si/SiGe MMIC's," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 705–714, Apr. 1995.

[4] H. Zirath, I. Angelov, N. Rorsman, C. Karlsson, and E. Kollberg, "A balanced W-band HFET doubler," in *Proc. 23rd European Microwave Conf.*, Madrid, Spain, Sept. 1993, pp. 837–839.

[5] Y. Kawasaki, K. Shirakawa, Y. Ohashi, and T. Saito, "A 30-to-60-GHz monolithic HEMT frequency doubler," in *Proc. 24th European Microwave Conf.*, Cannes, France, Sept. 1994, pp. 332–337.

[6] M. Funabashi, T. Inoue, K. Ohata, K. Maruhashi, K. Hosoya, M. Kuzuhara, K. Kanekawa, and Y. Kobayashi, "A 60 GHz MMIC stabilized frequency source composed of a 30 GHz DRO and a doubler," *IEEE MTT-S Int. Microwave Symp. Dig.*, Orlando, FL, May 14–19, 1995, pp. 71–74.

[7] H. J. De Los Santos, D. D. Nardi, K. L. Hargrove, M. Hafizi, and W. E. Stanchina, "High-efficiency InP-based DHBT active frequency multipliers for wireless communications," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 1165–1167, July 1996.

[8] D. A. Teeter, J. R. East, R. K. Mains, and G. I. Haddad, "Large-signal numerical and analytical HBT models," *IEEE Trans. Electron Devices*, vol. 40, pp. 837–845, May 1993.
[9] Q. M. Zhang, J. Hu, J. Sitch, R. K. Surridge, and J. M. Xu, "A new large signal HBT model," *IEEE MTT-S Int. Microwave Symp. Dig.*, San Diego, CA, May 23–27, 1994, pp. 1253–1256.
[10] A. Gruhle, H. Kibbel, U. König, U. Erben, and E. Kasper, "MBE-grown Si/SiGe HBT's with high β, f_t, and $f_{\max}$," *IEEE Electron Device Lett.*, vol. 13, pp. 206–208, Apr. 1992.
[11] G. M. Kull, L. W. Nagel, S.-W. Lee, P. Lloyd, E. J. Prendergast, and H. Dirks, "A unified circuit model for bipolar transistors including quasi-saturation effects," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 1103–1113, June 1985.
[12] C. Rauscher, "High-frequency doubler operation of GaAs field-effect transistors," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-31, pp. 462–473, June 1983.

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Moonil Kim (S'91–M'92), photograph and biography not available at the time of publication.

Frank J. Beißwanger, for a photograph and biography, see this issue, p. 667.

J.-F. Luy (M'86–SM'95), for a photograph and biography, see this issue, p. 570.

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